

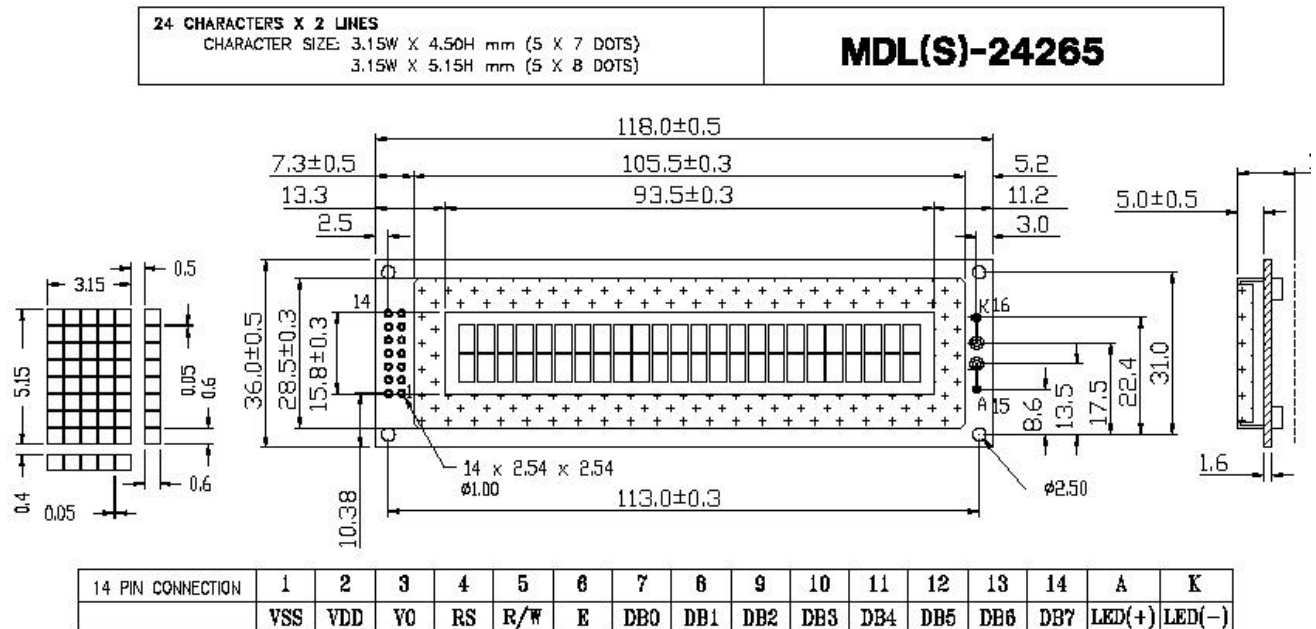
Displayansteuerung mit dem MC68332-Testboard

Nachdem wir die wichtigsten Befehle durchgenommen haben, ist es an der Zeit, mal eine Hardware-Bastelei zu machen. Aus Mangel an Testboards und Displays wird es ca. 3 Gruppen geben, die folgende Aufgaben zu lösen haben:

1. Untersuchen, wie ein Display an das Testboard angeschlossen werden kann (CS5 benutzen)
Hilfsmittel: Anschlussbelegung Stecker X1, Anschlussbelegung Display, Datenblätter
2. Bestimmen der Chip-Select-Registerinhalte gemäss Datenblatt MC68332
Das Display soll an Adresse \$400000 liegen.
3. Nach den ok vom Dozenten: Anschliessen des Displays an das Testboard
4. Nach dem ok vom Dozenten (und NUR dann): Speisung einschalten, Test
Das Controlregister muss mit \$33, \$3F, \$0F, \$01 beschrieben werden.
5. Schreiben einer Routine, die ein Zeichen auf das Display ausgibt
Nicht vergessen das Controlregister zu initialisieren. Busy-Flag abfragen!!! (Ask me!)
6. Schreiben einer Routine, die einen String aufs Display ausgibt
Beispiel: \$4A, \$41, \$4E, \$4E.
7. Schreiben einer Routine, die eine Dezimalzahl ausgibt
8. Schreiben eines Programms, das den Text „Sie haben Taste x gedrückt“ ausgibt

Fragen bitte jederzeit an den Dozenten. Viel Spass! Dauer: ca. 180 Minuten

Datenblatt Display (Anschlussbelegung)



VSS entspricht GND (bzw. 0V); VDD entspricht VCC (bzw. 5V).

V0 muss etwa 0,7V haben und wird mit einem Poti zwischen VCC und GND gewonnen (Kontrasteinstellung)

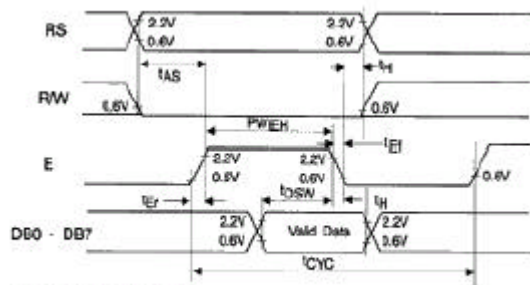
Das Signal E kann aus dem Chip-Select gewonnen werden (Timing-Diagramme beachten)

Anschlussbelegung des Steckers des Testboards. Des Stecker befindet sich auf der RAM/ROM Seite (Die mit den grossen, leeren Sockel).

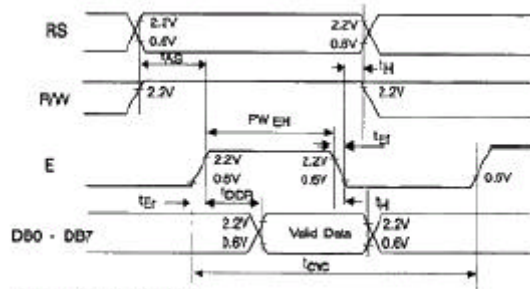
c	a
●	● 1
GND	GND
●	● 2
A10	A0
●	● 3
A11	A1
●	● 4
A12	A2
●	● 5
A13	A3
●	● 6
A14	A4
●	● 7
A15	A5
●	● 8
A16	A6
●	● 9
A17	A7
●	● 10
A18	A8
●	● 11
A19	A9
●	○ 12
R/W ₁	○ 13
○	○ 14
○	○ 15
○	○ 16
○	○ 17
○	/DGSL7
○	○ 18
○	/DGSE
○	○ 19
○	○ 20
●	● 21
D12	D8
●	● 22
D13	D9
●	● 23
D14	D10
●	● 24
D15	D11
○	● 25
○	/CS5
○	○ 26
○	○ 27
○	○ 28
○	○ 29
○	○ 30
●	● 31
VCC	VCC
●	● 32
GND	GND

X1

Timingdiagramm Display READ/WRITE

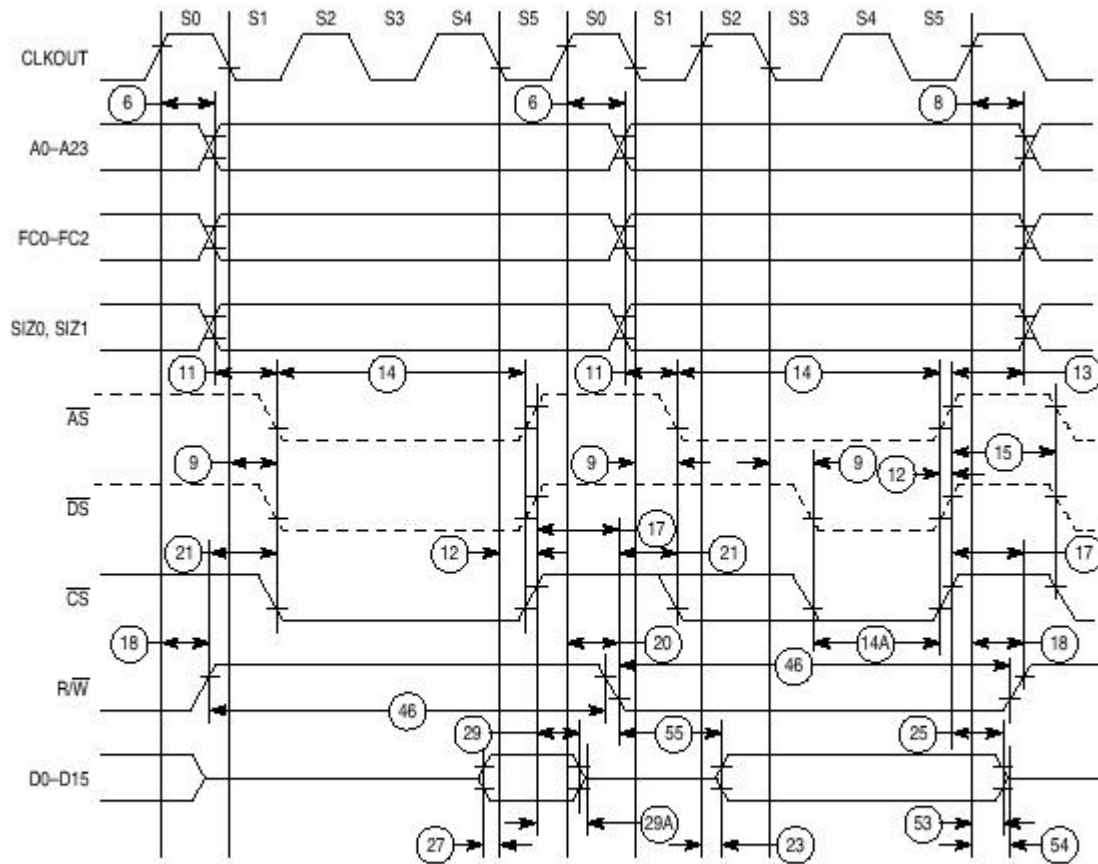


Write Operation



Read Operation

Timing-Diagramm des MC68332 READ/WRITE



NOTE: \overline{AS} and \overline{DS} timing shown for reference only.

88330 CHP SEL T1M

Figure A-11 Chip Select Timing Diagram

Informationen zum Bestimmen der Werte für die Chip-Select Register (CS5: FFFA60/FFFA62)

D.2.26 CSBAR[0:10] — Chip Select Base Address Registers \$YFFA4C–\$YFFA74

15	14	13	12	11	10	9	8	7	6	5	4	3	2	0
ADDR 23	ADDR 22	ADDR 21	ADDR 20	ADDR 19	ADDR 18	ADDR 17	ADDR 16	ADDR 15	ADDR 14	ADDR 13	ADDR 12	ADDR 11	BLKSZ	

RESET:

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Each chip-select pin has an associated base address register. A base address is the lowest address in the block of addresses enabled by a chip select. CSBARBT contains the base address for selection of a bootstrap peripheral memory device. Bit and field definition for CSBARBT and CSBAR[0:10] are the same, but reset block sizes differ.

ADDR[23:11] — Base Address

This field sets the starting address of a particular address space.

BLKSZ — Block Size

This field determines the size of the block above the base address that is enabled by the chip select.

Block Size Encoding		
BLKSZ[2:0]	Block Size	Address Lines Compared
000	2 K	ADDR[23:11]
001	8 K	ADDR[23:13]
010	16 K	ADDR[23:14]
011	64 K	ADDR[23:16]
100	128 K	ADDR[23:17]
101	256 K	ADDR[23:18]
110	512 K	ADDR[23:19]
111	1 M	ADDR[23:20]

D.2.28 CSOR[0:10] — Chip Select Option Registers \$YFFA4E–\$YFFA76

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODE	BYTE	R/W	STRB	DSACK				SPACE	IPL			AVEC			

RESET:

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Contain parameters that support bootstrap operations from peripheral memory devices. Bit and field definitions for CSORBT and CSOR[0:10] are the same.

MODE — Asynchronous Bus/Synchronous E-Clock Mode

Synchronous mode cannot be used with internally generated autovectors.

- 0 = Asynchronous mode selected
- 1 = Synchronous mode selected

BYTE — Upper/Lower Byte Option

The value in this field determines whether a select signal can be asserted.

R/W — Read/Write

This field causes a chip select to be asserted only for a read, only for a write, or for both read and write.

STRB — Address Strobe/Data Strobe

- 0 = Address strobe
- 1 = Data strobe

DSACK — Data Strobe Acknowledge

This field specifies the source of $\overline{\text{DSACK}}$ in asynchronous bus mode and controls wait state insertion.

SPACE — Address Space Select

This field selects an address space to be used by the chip-select logic.

IPL — Interrupt Priority Level

This field determines interrupt priority level when a chip select is used for interrupt acknowledgement. It does not affect CPU interrupt recognition.

$\overline{\text{AVEC}}$ — Autovector Enable

Do not enable autovector support when in synchronous mode.

0 = External interrupt vector enabled

1 = Autovector enabled

Option Register Function Summary							
MODE	BYTE	R/W	STRB	$\overline{\text{DSACK}}$	SPACE	IPL	$\overline{\text{AVEC}}$
0 = ASYNC	00 = Disable	00 = Rsvd	0 = $\overline{\text{AS}}$	0000 = 0 WAIT	00 = CPU SP	000 = All	0 = Off
1 = SYNC	01 = Lower	01 = Read	1 = $\overline{\text{DS}}$	0001 = 1 WAIT	01 = User SP	001 = Priority 1	1 = On
	10 = Upper	10 = Write		0010 = 2 WAIT	10 = Supv SP	010 = Priority 2	
	11 = Both	11 = Both		0011 = 3 WAIT	11 = S/U SP	011 = Priority 3	
				0100 = 4 WAIT		100 = Priority 4	
				0101 = 5 WAIT		101 = Priority 5	
				0110 = 6 WAIT		110 = Priority 6	
				0111 = 7 WAIT		111 = Priority 7	
				1000 = 8 WAIT			
				1001 = 9 WAIT			
				1010 = 10 WAIT			
				1011 = 11 WAIT			
				1100 = 12 WAIT			
				1101 = 13 WAIT			
				1110 = F term			
				1111 = External			

Control-Register des Displays:

Table 6 Instructions

Instruction	Code										Description	Execution Time (max) (when f_{op} or f_{osc} is 270 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	
Return home	0	0	0	0	0	0	0	0	1	—	Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 μ s
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 μ s
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DDRAM contents.	37 μ s
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	37 μ s
Set CGRAM address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM address. CGRAM data is sent and received after this setting.	37 μ s
Set DDRAM address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM address. DDRAM data is sent and received after this setting.	37 μ s
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 μ s

Instruction	Code										Description	Execution Time (max) (when f_{op} or f_{osc} is 270 kHz)		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0				
Write data to CG or DDRAM	1	0	Write data										Writes data into DDRAM or CGRAM.	37 μ s $t_{ADD} = 4 \mu$ s*
Read data from CG or DDRAM	1	1	Read data										Reads data from DDRAM or CGRAM.	37 μ s $t_{ADD} = 4 \mu$ s*

I/D = 1: Increment	DDRAM: Display data RAM	Execution time changes when frequency changes Example: When f_{op} or f_{osc} is 250 kHz, 37μ s $\times \frac{270}{250} = 40 \mu$ s
I/D = 0: Decrement	CGRAM: Character generator RAM	
S = 1: Accompanies display shift	ACG: CGRAM address	
S/C = 1: Display shift	ADD: DDRAM address	
S/C = 0: Cursor move	(corresponds to cursor address)	
R/L = 1: Shift to the right	AC: Address counter used for both DD and CGRAM addresses	
R/L = 0: Shift to the left		
DL = 1: 8 bits, DL = 0: 4 bits		
N = 1: 2 lines, N = 0: 1 line		
F = 1: 5 \times 10 dots, F = 0: 5 \times 8 dots		
BF = 1: Internally operating		
BF = 0: Instructions acceptable		

Note: — indicates no effect.

* After execution of the CGRAM/DDRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In Figure 10, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

Zeichensatz des Displays:

Upper 4 Bits Lower 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)			0@P`P							-	タ	ミ	α	ρ	
xxxx0001	(2)			!1AQa4							。	ア	チ	△	ä	q
xxxx0010	(3)			"2BRbr							「	イ	ツ	×	β	θ
xxxx0011	(4)			#3CScs							」	ウ	テ	モ	ε	∞
xxxx0100	(5)			\$4DTdt							、	エ	ト	ト	μ	Ω
xxxx0101	(6)			%5EUeu							・	オ	ナ	1	ε	Ü
xxxx0110	(7)			&6FVfv							ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)			'7GWgw							ア	キ	ヌ	ラ	g	π
xxxx1000	(1)			(8HXhx							イ	ク	ネ	リ	⌈	×
xxxx1001	(2))9IYiy							ウ	ケ	ル	ル	'	γ
xxxx1010	(3)			*:JZjz							エ	コ	ン	レ	j	≠
xxxx1011	(4)			+;K[k<							オ	サ	ヒ	ロ	*	斤
xxxx1100	(5)			,<L¥ll							カ	シ	フ	ワ	φ	円
xxxx1101	(6)			-=M]m}							ユ	ズ	ハ	ン	モ	÷
xxxx1110	(7)			.>N^n÷							ヨ	セ	ホ	ハ	ハ	
xxxx1111	(8)			/?O_0†							ッ	ソ	マ	マ	ö	■